

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE (USPTO)**

<b>Serial Number</b>	10/801,503
<b>Confirmation Number</b>	1822
<b>Filing Date</b>	March 15, 2004
<b>Title of Application</b>	Fractional-Type Phase-Locked Loop Circuit With Compensation of Phase Errors
<b>First Named Inventor</b>	Guido G. Albasini
<b>Assignee</b>	STMicroelectronics S.r.l. (large entity)
<b>Group Art Unit</b>	2611
<b>Examiner</b>	Khann C. Tran
<b>Attorney Docket Number</b>	2110-111-03
<b>Nature of the Office Communication to which this is responding</b>	Non-Final Office Action
<b>Date of the Office Communication</b>	September 15, 2008
<b>Nature of this Document</b>	Response to Non-Final Office Action

**CERTIFICATE OF MAILING OR TRANSMISSION**

I hereby certify that this correspondence is being transmitted via the Office electronic filing system, EFS-Web, addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 11<sup>th</sup> day of December 2008.

/Paola Kuvac/

Signature